CLAIMS

What is claimed is:

1. An intermediate microelectronic package, comprising:

a first encapsulated die assembly having an active surface and a back surface, said first encapsulated die assembly including at least one first microelectronic die having an active surface and at least one side and a first packaging material adjacent said at least one first microelectronic die side; and

a second encapsulated die assembly having an active surface and a back surface, wherein said second encapsulated die assembly back surface is attached to said first encapsulated die assembly back surface, said second encapsulated die assembly including at least one second microelectronic die having an active surface and at least one side and a second packaging material adjacent said at least one second microelectronic die side.

2. The intermediate microelectronic package of claim 1, wherein said first encapsulated die assembly active surface comprises said at least one first microelectronic die active surface and at least one surface of said first packaging material which is substantially planar to said first microelectronic die active surface.

3. The intermediate microelectronic package of claim 1, wherein said second encapsulated die assembly active surface comprises said at least one second microelectronic die active surface and at least one surface of said second packaging material which is substantially planar to said first microelectronic die active surface.

4. The intermediate microelectronic package of claim 1, further including at least one layer of dielectric material disposed over said first encapsulated die assembly active surface and at least one conductive trace extending through and residing on said at least one dielectric material layer.

5. The intermediate microelectronic package of claim 1, further including at least one layer of dielectric material disposed over said second encapsulated die assembly active surface and at least one conductive trace extending through and residing on said at least one dielectric material layer.

6. The intermediate microelectronic package of claim 1, further including an adhesive material disposed between said first encapsulated die assembly back surface and second encapsulated die assembly back surface.

7. The intermediate microelectronic package of claim 6, wherein said adhesive material is disposed in a desired patterned between said first encapsulated die assembly back surface and second encapsulated die assembly back surface.

8. The intermediate microelectronic package of claim 1, wherein said first and said second packaging material comprises an encapsulation material.

9. The intermediate microelectronic package of claim 1, wherein said first and said second packaging material comprises a microelectronic package core and an encapsulation material.

10. A method of fabricating microelectronic dice, comprising:

providing a first encapsulated die assembly having an active surface and a back surface, said first encapsulated die assembly including at least one first microelectronic die having an active surface and at least one side and a first packaging material adjacent said at least one first microelectronic die side; and

providing a second encapsulated die assembly having an active surface and a back surface, said second encapsulated die assembly including at least one second microelectronic die having an active surface and at least one side and a second packaging material adjacent said at least one second microelectronic die side; and

attaching said first encapsulated die assembly back surface to said second encapsulated assembly back surface.

11. The method of claim 10, further including forming at least one layer of dielectric material over said first encapsulated die assembly active surface.

12. The method of claim 11, further including forming at least one conductive trace extending through and residing on said at least one dielectric material layer.

13. The method of claim 10, further including forming at least one layer of dielectric material over said second encapsulated die assembly active surface.

14. The method of claim 13, further including forming at least one conductive trace extending through and residing on said at least one dielectric material layer.

15. The method of claim 10, further including simultaneously forming at least one layer of dielectric material over said first encapsulated die assembly active surface and at least one layer of dielectric material over said second encapsulated die assembly active surface.

16. The method of claim 15, further including simultaneously forming at least one conductive trace extending through and residing on said at least one dielectric material layer on said first encapsulated die assembly and at least one conductive trace extending through and residing on said at least one dielectric material layer on said second encapsulated die assembly.

17. The method of claim 10, wherein said attaching said first encapsulated die assembly back surface to said second encapsulated assembly back surface comprises disposing an adhesive on said first encapsulated die assembly back surface and contacting said second encapsulated assembly back surface with said adhesive.

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18. The method of claim 17, wherein said disposing an adhesive on said first encapsulated die assembly back surface comprises patterning said adhesive on said first encapsulated die assembly back surface.

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19. The method of claim 18, wherein said patterning said adhesive comprises placing at least one adhesive line between a first microelectronic die and an adjacent microelectronic die on said first encapsulated die assembly back surface.

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20. The method of claim 19, further including dicing said first encapsulated die assembly and said second encapsulated die assembly such that said dicing removes said at least one adhesive line.

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21. The method of claim 10, wherein said providing a first encapsulated die assembly comprises:

providing at least one first microelectronic die having an active surface and at least one side;

abutting a protective film against said at least one first microelectronic die active surface;

encapsulating said at least one microelectronic die with an encapsulation material adjacent said at least one first microelectronic die side, wherein said encapsulation material provides at least one surface of said encapsulation material substantially planar to said first microelectronic die active surface; and

removing said protective film.

22. The method of claim 10, wherein said providing a second encapsulated die assembly comprises:

providing at least one second microelectronic die having an active surface and at least one side;

abutting a protective film against said at least one second microelectronic die active surface;

encapsulating said at least one microelectronic die with an encapsulation material adjacent said at least one second microelectronic die side, wherein said encapsulation material provides at least one surface of said encapsulation material substantially planar to said second microelectronic die active surface; and

removing said protective film.

23. A method of fabricating a microelectronic package, comprising:

forming a first encapsulated die assembly comprising:

providing at least one first microelectronic die having an active surface and at least one side;

abutting a protective film against said at least one first microelectronic die active surface; and

encapsulating said at least one microelectronic die with an packaging material adjacent said at least one first microelectronic die side

to form a first encapsulated die active surface and a first encapsulated die back surface;

forming a second encapsulated die assembly comprising:

providing at least one second microelectronic die having an active surface and at least one side;

abutting a protective film against said at least one second microelectronic die active surface; and

encapsulating said at least one microelectronic die with an packaging material adjacent said at least one second microelectronic die side to form a second encapsulated die active surface and a second encapsulated die back surface; and

attaching said first encapsulated die assembly back surface to said second encapsulated assembly back surface.

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~~24~~. The method of claim ~~23~~, further including forming at least one layer of dielectric material over said first encapsulated die assembly active surface.

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~~25~~. The method of claim ~~23~~, further including forming at least one conductive trace extending through and residing on said at least one dielectric material layer.

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~~26~~. The method of claim ~~23~~, further including forming at least one layer of dielectric material over said second encapsulated die assembly active surface.

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27. The method of claim 23, further including forming at least one conductive trace extending through and residing on said at least one dielectric material layer.

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28. The method of claim 23, further including simultaneously forming at least one layer of dielectric material over said first encapsulated die assembly active surface and at least one layer of dielectric material over said second encapsulated die assembly active surface.

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29. The method of claim 28, further including simultaneously forming at least one conductive trace extending through and residing on said at least one dielectric material layer on said first encapsulated die assembly and at least one conductive trace extending through and residing on said at least one dielectric material layer on said second encapsulated die assembly.

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30. The method of claim 23, wherein said attaching said first encapsulated die assembly back surface to said second encapsulated assembly back surface comprises disposing an adhesive on said first encapsulated die assembly back surface and contacting said second encapsulated assembly back surface with said adhesive.

~~31~~ 22. The method of claim ~~30~~ 21, wherein said disposing an adhesive on said first encapsulated die assembly back surface comprises patterning said adhesive on said first encapsulated die assembly back surface.

~~32~~ 23. The method of claim ~~31~~ 22, wherein said patterning said adhesive comprises placing at least one adhesive line between a first microelectronic die and an adjacent microelectronic die on said first encapsulated die assembly back surface.

~~33~~ 24. The method of claim ~~32~~ 23, further including dicing said first encapsulated die assembly and said second encapsulated die assembly such that said dicing removes said at least one adhesive line.